RESPONSE UNDER 37 C.F.R. 1.116 EXPEDITED PROCEDURE EXAMINING GROUP 2822

Attorney Docket No. 5649-1206

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Gyu-Ho Lyu, et al.

Serial No.: 10/777,297 Filed: February 12, 2004

ed: February 12, 2004 ··· SEMICONDUCT

SEMICONDUCTOR DEVICES HAVING HIGH CONDUCTIVITY GATE

ELECTRODES

Date: November 21, 2007

Examiner: Ida M. Soward

Confirmation No.: 5272

Group Art Unit: 2822

Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL

Sir:

Applicants submit the present *Amendment After Final* in response to the *Final Office Action* ("*Final Action*") mailed September 27, 2007 to place the present application in condition for allowance.

It is not believed that an extension of time and/or additional fee(s) – including fees for net addition of claims – are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

In re: Gyu-Ho Lyu, et al.

Application Serial No.: 10/777,297

Filed: February 12, 2004

Page 2

Claim Listing:

Please replace all previous claim listings with the following claim listing.

1-11. (Cancelled)

12. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a gate line including a gate insulation pattern, a gate electrode that comprises a doped polysilicon layer and a metal silicide layer which are sequentially stacked on the semiconductor substrate;

a spacer formed on a sidewall of the gate line;

a conductive line pattern disposed on the gate line; and

an interlayer dielectric on the semiconductor substrate having a top surface that is coplanar with a top surface of the gate line;

wherein the conductive line pattern is parallel to the gate line and electrically connected to the gate electrode.

13-17. (Cancelled)

- 18. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern has at least the same length as the gate line.
- 19. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern is made of metal.
- 20. (Currently Amended) The semiconductor device of Claim [[14]]12, wherein the conductive line pattern bridges at least one gap in the metal silicide layer.
- 21. (Previously Presented) The semiconductor device of Claim 12, wherein the conductive line pattern decreases the resistance of the gate electrode.
 - 22. (Previously Presented) A semiconductor device comprising: